WHAT IS CLAIMED IS:

1. A method of controlling a cache memory connected to a main memory and divided into a plurality of cache blocks, which is executed by a computer that accesses the main memory through the cache memory, comprising the steps of:

supplying a lock/unlock signal to the cache memory to either set a replace-inhibition state of at least one of the cache blocks in which replacing said at least one of the cache blocks to the main memory is inhibited, or reset the replace-inhibition state of at least one of the cache clocks such that replacing said at least one of the cache block to the main memory is allowed; and

performing either reading or writing of the main memory by using the remaining cache blocks of the cache memory, other than said at least one of the cache blocks, such that, when the replace-inhibition state is set by the lock/unlock signal, replacing said at least one of the cache blocks to the main memory is inhibited during the reading or writing of the main memory.

2. The method according to claim 1, wherein, in said supplying step, at least one of flags corresponding to the cache blocks is set when the replace-inhibition state is set by the lock/unlock signal, and said at least one of the flags is reset when the replace-inhibition state is reset by the lock/unlock signal, and in said performing step, replacing the cache blocks, the flags of which are set, to the main memory is inhibited during the reading or writing of the main memory.

3. The method according to claim 1, wherein, when an all unlock instruction is supplied to the cache memory in said supplying step, all the replace-inhibition states of the cache blocks are reset by the all unlock instruction such that replacing all the cache blocks of the cache memory to the main memory is allowed.

4. A computer including a main memory and a cache memory, the cache memory being connected to the main memory and divided into a plurality of cache blocks, comprising:

a block state setting unit which supplies a lock/unlock signal to the cache memory to either set a replace-inhibition state of at least one of the cache blocks in which replacing said at least one of the cache blocks to the main memory is inhibited, or reset the replace-inhibition state of at least one of the cache clocks such that replacing said at least one of the cache block to the main memory is allowed; and

a reading/writing unit which performs either reading or writing of the main memory by using the remaining cache blocks of the cache memory, other than said at least one of the cache blocks, such that, when the replace-inhibition state is set by the lock/unlock signal supplied by the block state setting unit, replacing said at least one of the cache blocks to the main memory is inhibited during the reading or writing of the main memory.

5. The computer according to claim 4, wherein the block state setting unit sets at least one of flags corresponding to the cache blocks when setting the replace-inhibition state by the lock/unlock signal, and resets at least one of the flags corresponding to the cache blocks when resetting the replace-inhibition state by the lock/unlock signal, and wherein the reading/writing unit inhibits writing the cache blocks, the flags of

which are set by the block state setting unit, to the main memory during the reading or writing of the main memory.

6. The computer according to claim 4, wherein the block state setting unit is configured to supply an all unlock instruction to the cache memory when resetting all the replace-inhibition states of the cache blocks, so that writing all the cache blocks of the cache memory to the main memory is allowed.

7. A method of controlling a cache memory connected to a main memory and a peripheral system and divided into a plurality of cache blocks, comprising the steps of:

determining that an address designated by an instruction matches with an address of at least one of the cache blocks of the cache memory; and

supplying, when a lock/unlock instruction is received from a CPU and the match is determined, a lock/unlock signal to the cache memory to either set a replace-inhibition state of said at least one of the cache blocks in which replacing said at least one of the cache blocks to the main memory or the peripheral system is inhibited, or reset the replace-inhibition state of said at least one of the cache blocks such that replacing said at least one of the cache blocks to the main memory or the peripheral system is allowed.

8. A computer including a main memory and a cache memory, the cache memory being connected to the main memory and a peripheral system and divided into a plurality of cache blocks, comprising:

a comparator which determines that an address designated by an instruction matches with an address of at least one of the cache blocks; and

a lock/unlock control unit which supplies, when a lock/unlock instruction is received from a CPU and the match is determined by the comparator, a lock/unlock signal to the cache memory to either set a replace-inhibition state of said at least one of the cache blocks in which replacing said at least one of the cache blocks to the main memory or the peripheral system is inhibited, or reset the replace-inhibition state of said at least one of the cache blocks such that replacing said at least one of the cache blocks to the main memory or the peripheral system is allowed.

9. The computer according to claim 8, further comprising a load control unit which supplies, when a load instruction is received from the CPU and the match is determined by the comparator, a load signal to the cache memory to load data of said at least one of the cache blocks to the CPU.

10. The computer according to claim 8, further comprising a store control unit which supplies, when a store instruction is received from the CPU and the match is determined by the comparator, a store signal to the cache memory to store data from the CPU into said at least one of the cache blocks of the cache memory.

11. The computer according to claim 8, further comprising a flash control unit which supplies, when a flash instruction is

received from the CPU and the match is determined by the comparator, a flash signal to the cache memory to transfer data of said at least one of the cache blocks to the main memory or the peripheral system.

12. The computer according to claim 8, further comprising an invalidate control unit which supplies, when an invalidate instruction is received from the CPU and the match is determined by the comparator, an invalidate signal to the cache memory to invalidate said at least one of the cache blocks of the cache memory.

13. A method of controlling a cache memory that is connected to a main memory with a first address space and capable of acting as a random access memory, which is executed by a computer that accesses the main memory through the cache memory, comprising the steps of:

determining whether the cache memory is acting as the random access memory; and

assigning a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory.

14. The method according to claim 13, wherein the computer includes a bus control unit connecting the main memory and the cache memory, and a peripheral system connected to the computer through the bus control unit, and wherein, when the cache memory is acting as the random access memory and an access request

externally sent from an address outside the second address space of the cache memory is received, the computer accesses one of the main memory or the peripheral system instead of the cache memory.

15. A computer including a main memory and a cache memory, the main memory having a first address space and the cache memory being capable of acting as a random access memory, comprising:

a determination unit which determines whether the cache memory is acting as the random access memory; and

an assignment unit which assigns a second address space, which is separate from the first address space of the main memory, for the cache memory when the cache memory is acting as the random access memory.

16. The computer according to claim 15, further comprising a selection unit which selects one of a first assignment state and a second assignment state for the cache memory in response to a control signal, wherein, when the first assignment state is selected by the selection unit, the second address space is assigned for the cache memory, and when the second assignment state is selected by the selection unit, a third address space that partially overlaps the first address space is assigned for the cache memory.

17. The computer according to claim 15, further comprising:

a bus control unit connecting the main memory and the cache memory;

a peripheral system connected to the computer through the

bus control unit; and

an access control unit which accesses one of the main memory or the peripheral system instead of the cache memory when the cache memory is acting as the random access memory and an access request externally sent from an address outside the second address space of the cache memory is received.

add B3